Designing Next-Generation Real-Time Streaming Systems

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ABSTRACT

The design of next-generation systems running streaming applications is becoming extremely challenging as these systems are executing many real-time applications concurrently. To address this design challenge, predictable multi-processor systems-on-chip platforms and accompanying model-based design approaches are being developed. This tutorial presents an overview of future platforms and design approaches needed to design next-generation embedded systems for real-time streaming applications. During the hands-on session the participants apply this theory to a practical example.

Categories and Subject Descriptors

C.3 [**Special-Purpose and Application-Based Systems**]: Real-time and embedded systems,Signal processing systems

General Terms

Design, Performance, Reliability

Keywords

MPSoC, Composability, Predictability, Dataflow

1. INTRODUCTION

Novel embedded systems, such as smart phones, have to execute multiple streaming applications concurrently. A user may, for example, use a mobile phone to watch a video that is being decoded using an MPEG-4 decoder while an MP3 decoder is used to decode the accompanying audio. The applications may use an Internet connection that requires a software-defined radio protocol to download the required bit streams. The user expects that these applications have a robust behavior and that their performance is guaranteed. At the same time, the resource usage of these applications should be kept as small as possible in order to reduce cost both in terms of area and energy.

In the architecture domain there is a clear trend to use heterogeneous multi-processor systems-on-chip (MPSoCs) to meet the requirements of next-generation real-time streaming systems at an affordable area and energy cost. Designing these systems is a very challenging task, especially since the interactions between all hardware and software components need to be considered to provide timing guarantees. Predictable MPSoC platforms in combination with a model-based design approach based on the dataflow model-of-computation have emerged as a promising solution to address this design challenge. This tutorial presents a complete overview of the dataflow model-of-computation, a predictable MPSoC platform, and the model-based design approaches needed to design next-generation embedded systems for real-time streaming applications. The tutorial includes a hands-on session in which the participants apply this theory to a practical example.

2. OVERVIEW OF THE TUTORIAL

The tutorial focuses on the challenges involved in the design of systems that provide timing guarantees to streaming applications. It first discusses how modern streaming applications can be modeled and analyzed using the dataflow model-of-computation [7]. This process is illustrated using a state-of-the-art software-defined radio (SDR) application from industry [4]. Next, the tutorial shifts attention to the MPSoC platform. The speakers explain the design alternatives to consider in the development of a hardware platform that is to provide timing guarantees to streaming applications. The predictable and composable MPSoC (CoMPSoC) platform [2] from TU Eindhoven and the precision-timed (PRET) [3] architecture from UC Berkeley are used to show the audience practical example platforms that provide these timing guarantees. To successfully build a system, applications need to be mapped to these platforms under given timing constraints. The speakers first give an overview of existing timing-analysis techniques for dataflow graphs [1]. These techniques can be applied to applications modeled with a dataflow graph. The speakers further explain how hardware archictures and mapping decisions can be modeled in dataflow graphs and how, using the same timing-analysis techniques, the timing behavior of the mapped application can then be verified. These ingredients constitute a model-

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based design-flow that maps a timing-constrained application, expressed as a dataflow graph, onto an MPSoC [6]. The participants will experience such a mapping flow through a hands-on session within the tutorial. In this hands-on session, the participants use a state-of-the-art dataflow analysis and mapping tool [5] to experiment with all material taught in the tutorial. The tutorial concludes with a demonstration that shows a complete design flow, mapping the software-defined radio application introduced at the beginning of the tutorial onto the presented CoMPSoC platform.

The tutorial consists of the following sessions:

- (15 min.) Introduction to MPSoC design.
- (45 min.) Modeling and analyzing dynamic applications using the dataflow model-of-computation.
- (45 min.) Predictable MPSoC architectures.
- (30 min.) Automatic application mapping to predictable MPSoCs.
- (60 min.) Hands-on session using the SDF3 dataflow analysis and mapping tool set.
- (15 min.) Demonstration in which a SDR application is mapped and executed on the predictable CoMPSoC platform.

3. BIOGRAPHY OF THE SPEAKERS

Dr.ir. Sander Stuijk received his M.Sc. degree (with honors) in Electrical Engineering in 2002 and his Ph.D. degree in 2007 from the Eindhoven University of Technology. He is currently an assistant professor in the Department of Electrical Engineering at the Eindhoven University of Technology. Sander Stuijk has been working as a visiting researcher at the Technical University of Dortmund in Germany (2009). His research interests include modeling methods and mapping techniques for the design, specification, analysis and synthesis of predictable hardware/software systems.

Prof.dr.ir. Twan Basten is professor of computational models in the Department of Electrical Engineering of Eindhoven University of Technology and a research fellow of the Embedded Systems Institute, both in Eindhoven, the Netherlands. He received his Master's (with honors) and Ph.D. degrees in computing science from Eindhoven University of Technology in 1993 and 1998, respectively. He was a visiting researcher at the University of Waterloo, Canada, Philips Research Laboratories, Eindhoven, and Carnegie Mellon University, Pittsburgh. His research interests include the design of resource-constrained embedded systems, based on a solid mathematical foundation, with a focus on networked and multiprocessor systems. Twan Basten is and has been involved in several international research projects (FP5, FP6, and FP7), and several Dutch projects, also as a project leader. He has served (or is serving) in over 45 technical program committees. He (co)authored 1 book and over 120 scientific publications, of which four received a best paper award.

Dr. Benny Akesson got a M.Sc. degree in Computer Science and Engineering at Lund Institute of Technology, Sweden in 2005. In 2010, Dr. Akesson received his Ph.D. degree in Electrical Engineering at Eindhoven University of Technology on the topic of predictable and composable memory controllers. This research was conducted in collaboration with NXP Semiconductors. Dr. Akesson is currently extending his work as a postdoctoral researcher at Eindhoven University of Technology. His research interests include memory controller architectures, real-time resource scheduling, performance modeling, and virtualization.

Dr.ir. Marc Geilen received his M.Sc. degree (with honors) in Information Technology in 1996 and his Ph.D. in 2002, both from the Eindhoven University of Technology. He is currently an assistant professor in the electronic systems group and has been involved with different European IST projects and national research projects. He has been a visiting Mackay Professor at the EECS department at UC Berkeley in 2010. His research interests include validation and (formal) verification, modeling, simulation and programming paradigms for streaming systems and multi-dimensional optimization and trade-off analysis.

Orlando Moreira is a senior scientist at ST-Ericsson. He graduated in Electronics Engineering from the University of Aveiro. Before joining ST-Ericsson, he worked for Philips Research and NXP Semiconductors. In 2007-2008, he led a joint Nokia, NXP and ST-Ericsson team in developing a hard-real-time software architecture for radios. He published work on reconfigurable computing, real-time multiprocessor scheduling, and dataflow analysis.

Dr. Jan Reineke received a Bachelor's degree from the University of Oldenburg in 2003 and a Master's from Saarland University in 2005, both in Computer Science. In late 2008, he defended his Ph.D. thesis on ”Caches in WCET Analysis” at Saarland University. Since 2009, he is a postdoctoral scholar at the University of California, Berkeley in the group of Edward A. Lee. His research interests include timing predictability with a focus on the memory hierarchy, WCET analysis, and static analysis by abstract interpretation, in particular cache and shape analysis.

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