MAMPSX: A DEMONSTRATION OF RAPID, PREDICTABLE HMPSOC SYNTHESIS

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ABSTRACT

Heterogeneous Multiprocessor systems-on-chip (HMPSoC) are becoming popular as a means of meeting energy efficiency requirements of modern embedded systems. However, as these HMPSoCs run multimedia applications as well, they also need to meet real-time requirements. Designing HMPSoCs with predictable timing behavior is a key challenge, as the current design methods for these platforms are semi-automated, non-predictable, or support limited heterogeneity.

In this demonstration, we present a design framework to rapidly generate and implement predictable HMPSoC designs. It takes the application specifications and the architecture model as input and generates the entire HMPSoC, for FPGA prototyping, that meets the throughput constraints of the application. We also present results of a case study that computes the performance-power trade-offs of an industrial vision application. A tool-chain targeting the Xilinx Zynq FPGA is also presented.

1. INTRODUCTION

In this demonstration, we present MAMPSx — a design framework that takes application specifications and the architecture model as input and automatically generates the entire HMPSoC, together with corresponding software for processors and hardware accelerators, that meets the throughput constraints (Figure 1).

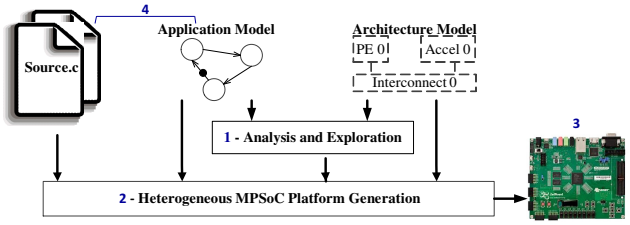

Fig. 1. MAMPSx Design Framework

Following are the key contributions of this demonstration:

1. An analysis and exploration stage, which provides a conservative bound on the performance using SDF3 [1].
2. A platform generation stage, for the rapid synthesis of predictable HMPSoCs that can be used for prototype based design space exploration.
3. A real-life demo of the framework targeting the Xilinx Zynq ZEDboard [2].
4. A case study on how our methodology can be used for fast design space exploration on the Xilinx Zynq heterogeneous platform, using an industrial vision application.

Interested readers may refer to [3] for the detailed description of the complete design framework.

2. EXPERIMENTAL RESULTS

To show the effectiveness of our design framework, we present a case study, using our design framework, to compute the trade-offs between execution time and power for an industrial vision application, called Fast Focus on Structures (FFoS) [4]. As shown in Figure 2, it consists of four main processing blocks. All processing blocks have software implementations, while *Projection*, *Erosion* and *Binarization* also have accelerator implementations. A mapping configuration is defined as a 3-tuple ($Proj_{type}$, $Eros_{type}$, Bin_{type}), where each $actor_{type}$ has value 0 or 1; for implementations on the ARM processor or as an accelerator, respectively.

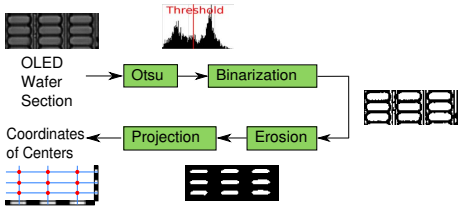

Fig. 2. FFoS Application

Figure 3 shows the execution time-power trade-offs for all eight configurations. All these configurations were generated in eight hours, including synthesis and implementation time.

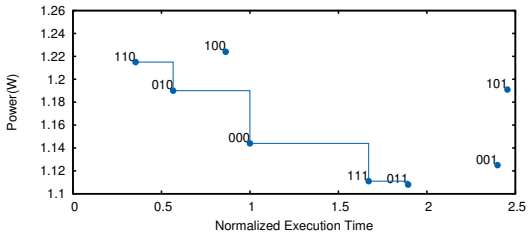

Fig. 3. Execution Time vs. Power Trade-offs

3. DEMONSTRATION

Our demonstrator presents the following three features of the design framework:

- Performance analysis of the FFoS application on the Zynq platform.
- Rapid exploration and generation of multiple mapping configurations for the application.
- Live demonstration of FFoS on the Zynq platform using a derived mapping configuration.

4. REFERENCES

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[4] Y. He, Z. Ye, D. She, B. Mesman, and H. Corporaal, "Feasibility analysis of ultra high frame rate visual servoing on FPGA and SIMD processor," in *Advanced Concepts for Intelligent Vision Systems*, 2011.